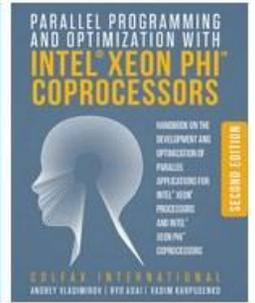


Parallel Programming and Optimization with Intel® Xeon Phi™ Coprocessors



Intel is offering an updated and expanded series of software developer trainings in parallel programming using the Intel® Xeon Phi™ coprocessors

This series of offerings provides software developers the foundation needed for modernizing their codes to extract more of the parallel compute performance potential found in both Intel® Xeon® processors and Intel Xeon Phi coprocessors.

A version of this series is being offered on Sept. 3 and 4 at Indiana University-Bloomington, where a new Intel Parallel Computing Center is being created. The courses contain materials and practical exercises appropriate for developers beginning their journey to parallel programming, as well as provide cutting-edge details to HPC experts on the best practices for Intel's multicore and many-core architectures and software development tools. The offerings include a one-day introductory seminar (CDT 101, free) and a one-day hands-on laboratory (CDT 102, free).

The training targets software engineers and architects, and covers the following topics:

- Intel Xeon Phi architecture: purpose, organization, pre-requisites for good performance, future technology
- Programming models: native, offload, heterogeneous clustering
- Parallel frameworks: automatic vectorization, OpenMP, MPI



For more information and to register for a workshop in your area, use the QR code or visit:
<http://tinyurl.com/2015ParallelProgrammingSeries>

Event Details:

Date: CDT 101: September 3, 2015 (CIB) Multipurpose Room A)
CDT 102: September 4, 2015 (CREST Ctr Conf Room)

Registration: 8:30 AM

Presentation: 9:00 AM to 4:00 PM

Location: Indiana University

9/3/15: 2709 E 10th Street
Bloomington, IN 47408

9/4 /15: CREST Center — Conference Room
420 N. Walnut St.
Bloomington, IN 47404

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**Cities are being continuously added, so check back often. Dates and cities are subject to change. Registrants will be notified of any changes via email.*