Statement of Work (SOW) for NPAC Subcontract

This SOW describes the work to be performed by NPAC under subcontract to the Syracuse Research Corporation (SRC) on the program proposed in response to Wright Laboratories PRDA Announcement SOL PRDA NO. 93-14-AAK "Development and Implementation of Computational Electromagnetics Techniques on Massively Parallel Computing Architectures"

1.0 SCOPE

The objective of this effort is to demonstrate the application of the Method of Moments on massively parallel processing (MPP) machines for prediction of RCS on full-scale material coated fighter aircraft. The effort will consist of two phases:

Phase I will be six months in length and will include adaptation of the existing PARAMOM code for an MPP environment. The performance and accuracy of the resulting MPP code will be demonstrated on specified EMCC benchmark targets. Scalability of the approach to larger problem sizes and larger MPP configurations will be demonstrated.

Phase II will be twelve months in length. The MPP code developed under Phase I will be refined and additional promising CEM techniques will be incorporated. The resulting code will be used to predict the RCS of a full-scale perfectly conducting VFY 218 fighter aircraft at relatively high frequencies (goal: 1 GHz), as well as the RCS of a 1/30 scale model of the VFY with a radar absorbing (RAM) coating at frequencies up to 1 GHz.

The products of the effort will include MPP implementations of PARAMOM under both phases I and II and written documentation of the algorithm and software development efforts.

2.0 APPLICABLE DOCUMENTS

PRDA Announcement SOL PRDA NO. 93-14-AAK

3.0 REQUIREMENTS

3.1 Task Breakdown

The tasks and subtasks of the proposed NPAC subcontract are described in this section. The major tasks are as specified in the PRDA announcement. Each major task is broken into subtasks which are specific to our proposed approach and to NPAC's contribution to the overall effort. The tasks for phases I and II are numbered separately as in the PRDA announcement.

PHASE I.

Task 1. Code Implementation on MPP

Under this task the SRC's general purpose MOM scattering code PARAMOM will be adapted for use on massively parallel processing systems. The parallelized code will be

implemented on a Thinking Machines CM5, an Intel Paragon, and an IBM SP-1. These codes will have identical CEM capabilities and source code structure, with appropriate differences in calls to the device-specific libraries and matrix solvers.

The emphasis in this task will be on parallelization of the matrix filling algorithm. Existing parallel matrix solution software will be used on each machine to perform direct (i.e. Gaussian elimination / LU decomposition) solution of the MOM matrix equations.

Subtask 1.1 Message Passing Algorithm Development

Under this task the MOM code will be adapted for use on MIMD machines which support the message passing (MP) paradigm. The task will involve problem partitioning, identification and mapping of data dependencies, and identification of necessary inter-node communication.

The parallelized MOM code will be implemented in f77 on the CM5 using the CMMD message passing library and ScaLAPACK parallel matrix solution routines. This implementation will be used to debug and tune the message passing approach. The implementation will emphasize portability and will serve as the basis for the optimized implementations developed under the subsequent subtasks.

Subtask 1.2 Implementation on CM5

The portable CM5 code developed under subtask 1.1 will be optimized for the CM5. This optimization will involve vectorization of the matrix filling code to take advantage of the CM5 nodes' vector processors and implementation in CMfortran (which is very similar to fortran90). The device-specific CMSSL matrix solution routines will be used.

Subtask 1.3 Implementation on Intel

The code developed under subtask 1.1 will be ported to, and optimized for, a 32 node iPSC/860. The code will use f77 with the NX message passing library, and either ScaLAPACK or ProSolver/DES for the matrix solution. This implementation will also run essentially unchanged on other Intel machines including Touchstone Delta and Paragon.

Subtask 1.4 Implementation on IBM SP1

The code developed under subtask 1.1 will be ported to, and optimized for, the IBM SP-1 using f77 and PVM (Parallel Virtual Machine) message passing, along with ScaLAPACK for matrix solution.

Task 2. Validation

NPAC will assist SRC in running the benchmark cases listed in the PRDA announcement on one of the parallel implementations, most likely the CM5, and in documenting the computational resources expended.

Task 3. Scalability and Performance Analysis

A scalability and performance analysis of the parallel MOM algorithm will be conducted. The scalability of the message-passing parallel implementation of PARAMOM will be analyzed from a theoretical viewpoint. The validity of the resulting scalablity model will be

demonstrated with empirical data resulting from test runs on several different MPP configurations.

Subtask 3.1 Analytic Scalability Analysis

Computational, memory, communication, and I/O loads will be determined analytically versus various parameters including problem size, number of nodes, node performance, and internode communication bandwidth. The scalability and performance characteristics of the matrix filling and matrix solution components will be analyzed separately. The results of this analysis will be, at a minimum:

a) a speedup curve (speedup versus number of nodes) for a realistic full-scale fighter problem on the CM5 and Paragon architectures. This curve will also be plotted as elapsed solution time versus number of nodes.

b) a curve of speedup versus problem size for a fixed number of nodes (chosen to correspond to machines which may be utilized in Phase II) on the two architectures.

Subtask 3.2 Empirical Validation of Scalability Model

The speedup curves developed under subtask 3.1 will be validated by empirical timings generated on machines available at NPAC, NAS, and through the CRPC. Available machines currently include 32, 128, and 1024 node CM5 configurations, 16 node Intel iPSC/860, 208 node Intel Sigma, Intel Paragon XP/S, and 8 node IBM SP-1.

PHASE II.

Task 1. Incorporation of Advanced Algorithms

NPAC will assist SRC in implementing advanced algorithms identified and/or formulated by SRC and incorporating the resulting code into the Phase I parallel MOM code.

Task 2. Parallel Code Development

Subtask 2.1 Out-of-Core Matrix Filling Algorithm Development

The parallel matrix filling code will be modified for out-of-core use on problems which are too large to fit in available local node memories. The out-of-core filling algorithm will be designed to accomodate block-oriented out-of-core matrix solvers.

Subtask 2.2 Identification of Target Platform for Large Scale Demo

A target machine will be chosen for the large scale deomstration. The choice will be made from among machines at NAS and at CRPC facilities and potentially others that SRC, NPAC, and the EMCC may jointly identify. The choice of machine will be made based on the results of the scalability and performance analysis of Phase I Task 3, as well as practical considerations such as machine availability, number of nodes, and available disk space.

Subtask 2.3 Optimization for Target Platform

The out-of-core PARAMOM matrix filling code will be optimized for efficiency on the chosen target platform's parallel file system (e.g. DataVault on CM5 or PFS on Paragon). The device-specific out-of-core filling and factoring algorithms (e.g. CMSSL or ProSolver/DES) will be tuned for optimum efficiency with the specific matrix sizes required by the full-scale demo cases.

Subtask 2.4 Validation of Final Code

NPAC will assist SRC in running the EMCC benchmark cases on the final MPP code.

Task 3. Large Scale Demonstration

RCS results for the VFY218 fighter aircraft will be demonstrated. RCS will be computed for the full-scale perfectly conducting target and for the 1/30 scale material-coated target. RCS results will be computed at a number of frequencies, with 1 GHz maximum frequency as a goal.

NPAC will assist SRC in scheduling and running the large scale demonstration cases.

Task 4. Software Evaluation

The MPP software development effort will be reviewed. All problems encountered and lessons learned will be described. Recommendations for future work in the CEM and parallel processing disciplines will be described.

3.2 Program Reviews

Program Reviews will be held at customer facilities or in conjunction with EMCC meetings in accordance with the PRDA announcement; including **for each phase**:

a) a theory/engineering review prior to code development
b) a midterm review after completion of prototype code
c) a final oral review

NPAC will present the technical status of their work at each Review.

3.3 Data Items

NPAC will provide bimonthly technical reports and contract fund status reports (CFSR) to SRC. NPAC will provide all presentation materials after Program Reviews. At the completion of each phase (i.e. Phase I and Phase II) NPAC will provide the following reports as described in the PRDA announcement:

- Theory Manual describing the theory and algorithm development; draft due 2 weeks before first review meeting in each phase.

- Installation and Porting Guide ; draft due 2 weeks before midterm review meeting in each phase.

- Final Report summarizing technical work done; draft due 2 weeks prior to the final oral review in each phase.

The final version of each report is due two months after the completion of the each phase.

In addition NPAC will assist SRC in preparation of the User's Manual.

3.4 Products

All software developed under this effort will be delivered with unlimited rights to SRC. Source code will be provided on magnetic media.