C: Paper Number: C459

Paper Title: "A Parallel Viterbi Decoding Algorithm"

Author(s): J. S. Reeve

Referee Code:

Referee:

Name: David W. Walker

Address: Oak Ridge National Laboratory
P. O. Box 2008
Oak Ridge TN 37831-6367
USA

Signature:

Referee Recommendations. Please indicate overall recommendations here and details in following sections

e.g. (1) publish as is

(2) accept provided changes suggested are made

(3) reject

D: REFEREE'S COMMENTS (For Editor Only)

Paper number: C459 Referee Code:

As far as I can tell this is a sound paper. However, it is difficult to be certain as the paper is only really comprehensible to an expert on Viterbi decoding. The paper should be lengthened in an effort should be made to make it of interest to a wider readership.

E: REFEREE'S COMMENTS (For Author and Editor)

Paper number: C459 Referee Code:

This paper would greatly benefit from a more detailed explanation of the Viterbi algorithm. Many readers will not be familiar with how to interpret some of the figures, particularly Figures 1 and 2. Also, given that memory is presented as the prime reason for wanting a parallel algorithm, it would be useful to know what lengths of the generating shift register are typical in applications, and how strong the motivation is to go to greater lengths. This would allow the potential impact of the parallel algorithm to be assessed.

In the summary section, the author says that the timing difference between the just communication in the parallel algorithm and the complete parallel algorithm is always less than 5%. This means that more than 95% of the time in the parallel algorithm is spent on communication. This doesn't seem to be borne out by the results shown in the tables. For example, in Table IV for the code (127,106,7) the time on one processor is 259 seconds and on four processors is 174 seconds. This would imply that the time spent on communication is $174 - 259/4 = 109.25$ seconds, which is only about 63% of the total time.

Can the use of FPGA technology address the large memory requirements of the Viterbi algorithm mentioned in the second paragraph of the introduction?

There are a couple of minor issues that need to be addressed.

1. In line 6 of the introduction the word "codes" is repeated.
2. In Figure two the text says that thick lines are used to show path branches for input bit 0. All the lines look the same thickness to me. The only difference is that some of the arrow heads are larger than others.
3. The text says that Figure 3 shows the matrix for BCH (15,7,2), whereas the figure caption says it shows the matrix for BCH (31,16,7).

F: Presentations Changes

Paper number: C459 Referee Code:

Title Changes:

Abstract Changes:

Reference Changes/Additions:

Other Comments (Grammar, etc.):