A History of Parallel Computing

This document is a timeline of major developments in parallel computing. It will eventually appear as part of a textbook on parallel programming, but might also be separately published. All contributions and corrections are welcomed, and should be sent to `gregw@cs.anu.edu.au`.

The persons listed below have contributed or corrected articles; I am particularly grateful to Michael Wolfe, whose generous early assistance got this off the ground, and to Eugene Miya, who provided many useful pointers.

TA	Tamir Azaz	`tamir@meiko.co.uk`
JB	John Bennett	`jbennett@ncube.com`
EAB	Edward Bertsch	`eab@msc.edu`
BMB	Bruce Boghosian	`bmb@think.com`
BRC	Brad Carlile	`bradc@cray.com`
WD	Bill Dally	`billd@ai.mit.edu`
JD	Jack Dongarra	`dongarra@cs.utk.edu`
JF	John Feo	`feo@diego.llnl.gov`
JMF	Jim Flemming	`flemming@vino.enet.dec.com`
WH	Willi Hasselbring	`willi@informatik.uni-essen.de`
RWH	Roger Hockney	`rwh@pac,soton.ac.uk`
RJ	Rick Johnson	`rickj@ssd.intel.com`
LSK	Larry Kaplan	`lkaplan@ultra.tera.com`
HGK	Harwood Kolsky	`harwood@cse.ucsc.edu`
VK	Venkata Konda	`vkonda@ncube.com`
CEL	Charles E. Leiserson	`cel@theory.lcs.mit.edu`
TL	Tom Lovett	`tdl@sequent.com`
BM	Barry Margolin	`barmar@think.com`
LFM	Larry Meadows	`lfm@pgroup.com`
ENM	Eugene Miya	`eugene@wilbur.nas.nasa.gov`
YO	Yoshio Oyanagi	`oyanagi@is.s.u-tokyo.ac.jp`
SCP	Stephen C. Perrenod	`perrenod@renaissance.cray.com`
RR	Robert Rau	`rau@hplabs.hpl.hp.com`
JRR	James R. Reinders	`reinders@ssd.intel.com`
PR	Paul Repacholi	`zrepachol@cc.curtin.edu.au`
MS	Matthias Schumann	`schumann@informatik.tu-muenchen.de`
MCS	Markus Schwehm	`schwehm@immd7.informatik.uni-erlangen.de`
DHS	Dave Shaver	`shaver@convex.com`
RS	Roger Shepherd	`roger@inmos.co.uk`
MKS	Mark Smotherman	`mark@cs.clemson.edu`
DS	Douglas E. Solomon	`doug@sgi.com`
HSS	Harold Stone	`hstone@sunset.ee.cornell.edu`
PDT	Philip Tannenbaum	`b47tbaum@sx.iah.nec.com`
PGW	Paul Whiting	`pgw@mel.dit.csiro.au`

GVW	Greg Wilson	gvw@epcc.ed.ac.uk
MW	Mike Wolfe	mwolfe@cse.ogi.edu

1956

IBM starts 7030 project (known as STRETCH), with the goal of producing a machine with 100 times the performance of the IBM 704, initiated by Atomic Energy Commission at Los Alamos. (MW,HGK: IBM, STRETCH.)

1958

Bull of France announces the Gamma 60 with multiple function units and fork and join operations in its instruction set; 19 are later built. (MKS: Bull, Gamma 60.)

1959

IBM delivers first STRETCH computer. Only seven are ever built, but much of the techology re-surfaces in the later IBM 7090 and 7094. (MW,HGK: IBM, STRETCH.)

1960

Control Data starts development of CDC 6600. (MW: CDC, Cray, CDC 6600.)

1962

C. A. Petri describes Petri Nets. (WH: Petri, Petri-Nets.)

1964

Atomic Energy Commission urges manufacturers to look at "radical" machine structures. This leads to CDC Star-100, TI ASC, and Illiac-IV. (MW: AEC, CDC, TI, Illiac.)

Control Data Corporation produces CDC 6600, the world's first commercial supercomputer. (GVW: CDC, Cray, CDC 6600.)

Air Force signs Illiac-IV contract with University of Illinois. The project is led by Daniel Slotnick; primary subcontractors are Burroughs and Texas Instruments. (MW: Illiac-IV.)

1965

IBM 2938 Array Processor delivered. A programmable digital signal processor, it proves very popular in the petroleum industry. (HGK: IBM, IBM 2938, array processor.)

Multics project begun by GE, MIT, and AT&T Bell Laboratory, to develop a general-purpose shared-memory multiprocessing timesharing system. (BM: GE, MIT, Bell Labs, Multics, symmetric multiprocessing.)

1966

Bernstein introduces Bernstein's Condition for statement independence, which is foundation of subsequent work on data dependency analysis. (GVW: Bernstein, compilation, data dependency.)

Flynn publishes paper describing architectural taxonomy. (GVW: Flynn, taxonomy.)

1967

Amdahl publishes paper questioning feasibility of parallel processing; his argument is later called “Amdahl's Law”. (GVW: Amdahl.)

IBM produces the 360/91 (later model 95) with dynamic instruction reordering. 20 of these were produced over the next several years; the line was eventually replaced with the slower Model 85. (MW,HGK: IBM, IBM 360/91.)

1968

Edsger Dijkstra describes semaphores. (GVW: Dijkstra, semaphore.)

Duane Adams of Stanford University coins the term “dataflow” while describing graphical models of computation in his Ph.D thesis. (PGW: dataflow, Stanford University.)

Honeywell delivers first Multics system (symmetric multiprocessor with up to 8 processors). (BM: Honeywell, Multics, symmetric multiprocessing.)

Group formed at Control Data to study computing needs for image processing; this leads to AFP and Cyberplus designs. (MW: CDC, Cyberplus.)

1969

CDC produces CDC 7600 pipelined supercomputer. (GVW: CDC, Cray, CDC 7600.)

1970

Floating Point Systems Inc. founded by former C N Winningstad and Tektronix employees to manufacture floating-point co-processors for minicomputers. (GVM,BRC: FPS.)

PDP-6/KA10 master/slave (asymmetric) multiprocessor jointly developed by MIT and DEC. (JMF: DEC, asymmetric multiprocessor.)

Development of C.mmp begins at Carnegie-Mellon. (GVW: C.mmp, CMU.)

1971

Edsger Dijkstra poses the dining philisophers problem which is often used to test the expressivity of new parallel languages. (WH: Dijkstra, dining philisophers.)

Intel produces 4004 microprocessor (world's first single-chip CPU). (GVW: Intel.)

CDC delivers hardwired Cyberplus parallel radar image processing system to Rome Air Development Center, where it produces 250 times the performance of CDC 6600. (MW: CDC, Cyberplus.)

Texas Instruments delivers the Advanced Scientific Computer (also called Advanced Seismic Computer). Seven of these machines were developed. An aggressive automatic vectorizing Fortran compiler was developed for this machine. (MW: TI, ASC.)

1972

Seymour Cray leaves Control Data Corporation, founds Cray Research Inc. (GVW: CDC, CRI.)

Quarter-sized (64 PEs) ILLIAC-IV installed at NASA Ames. (GVW: Illiac-IV, NASA Ames.)

BBN builds first Pluribus machines as ARPAnet switch nodes. (GVW: BBN, Pluribus.)

Goodyear produces STARAN, a 4×256 1-bit PE array processor using associative addressing and a FLIP-network. (MCS: Goodyear, Staran.)

Burroughs builds PEPE (Parallel Element Processor Ensemble) with 8×36 processing elements and associative adressing. (MCS: Burroughs, PEPE.)

Paper studies of massive bit-level parallelism done by Stewart Reddaway at ICL. These later lead to development of ICL DAP. (GVW: ICL, DAP.)

TOPS-10 monitor for PDP-10 re-written by DEC to allow asymmetric multiprocessing. (JMF,PR: DEC, asymmetric multiprocessor.)

1974

Tony Hoare describes monitors. (GVW: Hoare, monitors.)

Jack Dennis and David Misunas at MIT publish first paper describing a dataflow computer. (PGW: MIT, dataflow.)

IBM 3838 array processor (a general-purpose digital signal processor) delivered. (HGK: IBM, IBM 3838, array processor.)

Work begins on prototype DAP (Distributed Array Processor) at ICL. (GVW: ICL, DAP.)

Design begins on Burroughs Scientific Processor (BSP). (MW: BSP.)

Burton Smith begins designing context-flow Heterogeneous Element Processor (HEP) for Denelcor. (GVW: Denelcor, HEP.)

The IBM language VECTRAN, a major input to FORTRAN 8X, developed for the 3838. (HGK: IBM, VECTRAN, FORTRAN.)

1975

Edsger Dijkstra describes guarded commands. (WH: Dijkstra, guarded commands.)

Illiac-IV becomes operational at NASA Ames after concerted check out effort. (MW: Illiac-IV.)

Work begins at Carnegie-Mellon University on Cm*, with support from DEC. (GVW: CMU, Cm*.)

Design of iAPX 432 (symmetric multiprocessor) begins at Intel. (GVW: Intel, iAPX 432.)

Cyber 200 project begins at Control Data. (MW: CDC, Cyber.)

1976

First Cray-1 delivered to Los Alamos National Laboratory. (MW: CRI, Cray-1.)

Borroughs delivers PEPE to BMDATC Advanced Research Center, Huntsville, Alabama (MCS: Goodyear, PEPE.)

Control Data delivers Flexible Processor, a programmable signal processing unit. (MW: CDC, Flexible Processor.)

Floating Point Systems Inc. delivers 38-bit AP-120B array processor that issues multiple pipelined instructions every cycle. (BRC: FPS, array processor, LIW.)

Floating Point Systems Inc. describes loop wrapping, later called software pipelining, to program pipelined multiple instruction issue processors. (BRC: FPS, software pipelining, array processor.)

1977

Roger Hockney introduces $n_{1/2}$ and r_∞ as metrics for pipelined and other architectures. (RWH: $n_{1/2}$, r_∞, performance metrics.)

C.mmp hardware completed at Carnegie-Mellon University (crossbar connecting minicomputers to memories). (GVW: CMU, C.mmp.)

Al Davis of the University of Utah, in collaboration with the Burroughs Corporation, builds the first operational hardware dataflow processor called the DDM1 (Data-Driven Machine 1). This is based on the static model of dataflow token scheduling. (PGW: Davis, University of Utah, Burroughs Corporation, DDM1, static dataflow.)

Massively Parallel Processor project first discussed at NASA for fast image processing. (MW: Goodyear, MPP.)

Defacto standards activity started by the linear algebra community to define basic vector operations used in linear algebra. The collection is called the Basic Linear Algebra Subprograms or BLAS. Later the name is changed to the Level 1 BLAS. Project to develop a portable software package used to solve systems of linear equation is started, this effort is called the LINPACK project. (JD: BLAS, standards, LINPACK.)

1978

Fortune and Wyllie publish paper describing the PRAM model. (GVW: Fortune, Wyllie, PRAM.)

Kung and Leiserson published first paper on systolic arrays. (CEL: systolic arrays.)

Leslie Lamport describes algorithm for creating partial order on distributed events. (GVW: Lamport, virtual time.)

Tony Hoare describes CSP. (WH: Hoare, CSP.)

John Backus (inventor of Fortran) publishes paper on FP systems, arguing that dependence on conventional languages has made the development and use of non-von Neumann architectures uneconomical, and has deprived computer architects of an intellectual foundation for new computers. (PGW: Backus, FP, dataflow.)

Arvind, Kim Gostelow and Wil Plouffe (at the University of California, Irvine) describe the Unravelling Interpreter (U-Interpreter), which exploits even greater concurrency than the static dataflow model. This idea comes to be referred to as the dynamic dataflow model. The dataflow language Id (Irvine dataflow) is introduced. (PGW: Arvind, Gostelow, Plouffe, U-Interpreter, dynamic dataflow, Id.)

BBN begins design of distributed-shared memory machine based around "butterfly" switch, with its roots in work on perfect-shuffle networks by Stone (1972) and on Omega networks by Lawrie (1975). (GVW, HSS: BBN, Butterfly.)

1979

Parviz Kermani and Leonard Kleinrock describe the virtual cut-through technique for message routing. (GVW: Kermani, Kleinrock, virtual cut-through, message routing.)

ICL DAP delivered to Queen Mary College, London — world's first commercial massively parallel computer. (GVW: ICL, DAP.)

Inmos set up by British government to develop and produce memory chips and microprocessors. (GVW: Inmos.)

First single-processor prototype of Denelcor HEP operational. (GVW: Denelcor, HEP.)

The first dataflow multiprocessor (with 32 processors) becomes operational at CERT-ONERA in Toulouse, France. It is based on the static model and is known as the LAU system after its programming language (Language en Assignation Unique). (PGW: dataflow, CERT-ONERA, LAU.)

Texas Instruments begins work on the DDP (Data-Driven Processor), based on the static model, and on a FORTRAN compiler to run on it. (PGW: dataflow, TI, DDP.)

IBM's John Cocke designs the 801, the first of what are later called RISC architectures. (HGK: IBM, RISC, IBM 801.)

Level 1 BLAS published/released. LINPACK software package complete and released; the LINPACK Users' Guide finished; the Linpack Users' Guide contains the first LINPACK Benchmark Report, with 17 machines ranging from the DEC PDP-10 to the Cray 1 which achieves 4 MFLOPS for a 100^2 matrix at full precision on a single processor. (JD: BLAS, standards, Linpack Benchmark, Cray-1.)

1980

J. T. Schwartz publishes paper describing and analysing the ultracomputer model, in which processors are connected in a shuffle/exchange graph. (HSS: Schwartz, ultracomputer.)

Teradata spun off from Citibank to develop parallel database query computers. (GVW: Teradata.)

Burroughs Scientific Processor project cancelled after one sale but before delivery. (MW: BSP.)

Mitsui Shipbuilding Company installs a 32-processor ring array called PPA at Hokkaido University, Japan. (YO: PPA.)

DEC develops KL10 TOPS-10 based symmetric multiprocessor (up to three CPUs supported, but a customer built a five-CPU system). (JMF: DEC, symmetric multiprocessor.)

1981

Franco Preparata and Jean Vuillemin describe the cube-connected cycles topology. (GVW: Preparata, Vuillemin, cube-connected cycles.)

Carver Mead gives seminar on massive parallelism at California Institute of Technology; inspires development of Cosmic Cube hypercube at Caltech by group led by Charles Seitz (computer science) and Geoffrey Fox (physics). (GVW: Caltech, hypercube, Seitz, Fox.)

First BBN Butterfly delivered — 68000s connected through multistage network to disjoint memories, giving appearance of shared memory. (GVW: BBN, Butterfly.)

iAPX 432 prototype completed; Intel abandons project. (GVW: Intel, iAPX 432.)

DEC produces VAX 11/782 asymmetric multiprocessor; a small number of 4-processor machines (11/784) are built. (JMF, PR: DEC, VAX, asymmetric multiprocessor.)

Control Data delivers Cyber 205 vector supercomputer. (MW: CDC, Cyber.)

The first dynamic dataflow computer becomes operational at the University of Manchester. (PGW: Manchester, dataflow.)

Floating Point Systems Inc. delivers 64-bit FPS-164 array processor that issues multiple pipelined instructions every cycle, start of mini-supercomputer market. (BRC: FPS, FPS-164, array processor, LIW, mini-supercomputer.)

Silicon Graphics Inc. is founded in late 1981, by James H. Clark and others to develop the IRIS, a high-performance graphics workstation. (DS: Silicon Graphics, IRIS, Clark.)

1982

Illiac-IV decommissioned. (GVW: Illiac-IV.)

Steve Chen's group at Cray Research produces first X/MP machine (2 pipelined processors with shared memory). (GVW: CRI, Cray-X/MP.)

First Denelcor HEPs installed in US. (GVW: Denelcor, HEP.)

Hitachi introduces S-810/10 and S-810/20 vector supercomputers. (YO: S-810, Hitachi.)

Control Data improves Flexible Processor to make Advanced Flexible Processor. (MW: CDC, AFP.)

Cosmic Cube hypercube prototype operational at Caltech; first predecessor of CrOS (Crystalline Operating System) running. (GVW: Caltech, hypercube, MPI.)

Convex founded to pursue mini-supercomputer market. (GVW: Convex.)

Alliant founded (GVW: Alliant.)

1983

DARPA starts Strategic Computing Initiative, which helps fund such machines as Thinking Machines Connection Machine, BB&N Butterfly, WARP from Carnegie Mellon University and iWarp from Intel Corp. (MW: DARPA.)

Gottlieb and others describe the NYU Ultracomputer, a shared-memory machine based on a multistage network using message combining. Works begins on construction of the Ultracomputer at New York University; a related project, the RP3, is begun at IBM. (AG: message combining, NYU, Ultracomputer, RP3, IBM.)

Full Cosmic Cube hypercube running at Caltech; work begins on Mark II. Steve Colley and John Palmer (of Intel) sees Caltech machines, and leaves Intel to found nCUBE. (GVW,VK: Caltech, hypercube, nCUBE.)

Fujitsu ships first VP-200 vector supercomputer. (YO: Fujitsu, VP-200.)

NEC introduces SX-1 vector supercomputer. (YO: NEC, SX-1.)

Massively Parallel Processor delivered by Goodyear Aerospace to NASA Goddard. (MW: Goodyear, MPP.)

Loosely-coupled VAXclusters supported by DEC's VMS operating system. (JMF: DEC, symmetric multiprocessor, VAX.)

Myrias Research founded as spin-off from University of Alberta to build shared-memory mini-supercomputers. (GVW: Myrias.)

Scientific Computer Systems founded to design and market a Cray-compatible minisupercomputer. (MW: SCS.)

Sheryl Handler and Danny Hillis found Thinking Machines Corporation; Danny Hillis' Ph.D. thesis becomes the starting point for a massively-parallel AI supercomputer. (BMB: TMC.)

ETA Systems, Inc. spun off from CDC to develop a new generation of vector supercomputers. (GVW: CDC, ETA.)

Encore founded. (GVW: Encore.)

Sequent founded. Several of its founders are former members of Intel iAPX 432 project. (GVW,TL: Sequent, Intel, iAPX 432.)

Cray-1 with 1 processor achieves 12.5 MFLOPS on 100^2 LINPACK. (JD: Linpack Benchmark, Cray-1.)

David May publishes first description of Occam, a concurrent programming language closely associated with the transputer. (RS: Occam.)

Sisal 1.0 (Streams and Iterations in a Single-Assignment Language) language definition released by Lawrence Livermore National Laboratory (LLNL), Colorado State University, DEC, and University of Manchester. A derivative of VAL, the language included array operations, streams, and iterations. (JF: SISAL, functional languages.)

1984

Kurt Mehlhorn and Uzi Vishkin describe how various classes of PRAM can simulate one another. This work forms the basis for Valiant's later work on random routing and optimality. (GVW: Mehlhorn, Vishkin, PRAM, emulation.)

Cydrome founded to build VLIW-style mini-supercomputers with architectural support for software pipelining of loops. (RR: Cydrome, VLIW.)

Sequent produces first shared-memory Balance multiprocessors, using NS32016 microprocessors and proprietary DYNIX symmetric operating system. (GVW,TL: Sequent, Balance.)

Mitsui Shipbuilding Company installs a two-dimensional toroidal array of processors, PAX-64J, at the University of Tsukuba, Japan. (YO: PAX-64J.)

Cray X/MP family expanded to include 1 and 4 processors. (GVW: CRI, Cray-X/MP.)

Convex ships prototype version of C1 mini-supercomputer. (DHS: Convex, C1.)

Unimpressed with available commercial machines, Caltech begins work on Mark III hypercube. (GVW: Caltech, hypercube.)

Intel Scientific Computers set up by Justin Rattner to produce commercial hypercube machines. (GVW: Intel, hypercube.)

Multiflow founded by Fisher and others from Yale to produce very long instruction word (VLIW) supercomputers. (GVW: Multiflow.)

Cray X/MP with 1 processor achieves 21 MFLOPS on 100^2 LINPACK. (JD: Linpack Benchmark, Cray X/MP.)

1985

Dally and Seitz develop model of wormhole routing, invent virtual channels, and show how to perform deadlock-free routing using virtual channels. (WD: Dally, Seitz, wormhole routing, virtual channels.)

Leiserson publishes first paper describing fat-tree network. (CEL: fat trees, message routing.)

Pfister and Norton analyse effect of hot spots in multistage networks, and describe how message combining can ameliorate their effect. (GVW: Pfister, Norton, hot spots, message combining.)

TMC demonstrates first CM-1 Connection Machine to DARPA. (BMB: TMC, CM-1.)

Denelcor closes doors. (GVW: Denelcor.)

IBM introduces 3090 vector processor. (HGK: IBM, IBM 3090.)

Intel produces first iPSC/1 hypercube (80286 processors connected through Ethernet controllers). (GVW: Intel, iPSC/1.)

Inmos produces first (integer) T414 transputer. Members of implementation group leave to found Meiko, which demonstrates its first transputer-based Computing Surface at SIGGRAPH that year. ESPRIT Supernode project begun to produce floating-point transputer. (GVW: Inmos, transputer, Supernode, Meiko.)

Alliant delivers first FX/8 vector multiprocessor machines using a custom implementation of an extended Motorola 68020 instruction set. An auto-parallelizing Fortran compiler is shipped with the machine. (SCP: Alliant, FX/8.)

Fujitsu introduces VP-400 vector supercomputer. (YO: Fujitsu, VP-400.)

First NEC SX-2 vector supercomputer shipped (6.0 ns clock, capable of producing 8 floating point results per clock cycle, up to 256 MByte memory). (PDT: NEC, SX-2.)

nCUBE produces first nCUBE/10 hypercube using custom processors. (GVW: nCUBE, nCUBE/10.)

Teradata ships first DBC/1012 parallel database query engine (Intel 8086 processors connected by proprietary tree network). (GVW: Teradata, DBC/1012.)

Ring-connected multiprocessor delivered by Control Data, called the Cyberplus. (MW: CDC, Cyberplus.)

Floating Point Systems Inc. delivers FPS-264, an ECL version of 64-bit FPS-164 array processor that issues multiple pipelined instructions every cycle. (BRC: FPS, FPS-264, array processor, mini-supercomputer.)

Convex ships first production version of single-processor C1 mini-supercomputer. (MW,DHS: Convex, C1.)

Cray Research produces Cray-2, with four background processors, a single foreground processor, and a 4.1 nsec clock cycle. (GVW: CRI, Cray-2.)

IBM begins RP3 project, intending to build a scalable shared-memory multiprocessor using a message-combining switch. (HGK: IBM, IBM RP3.)

Stellar Computer, Inc., founded by Bill Poduska, former Apollo Computer founder, to build single-user high-performance graphics workstations. (MW: Stellar.)

Ardent Computer founded by Allen Michels, former founder of Convergent Technologies, and Gorden Bell, formerly of DEC, to build machines in competition with Stellar. (MW: Ardent.)

Supertek Computers, Inc. is founded by Mike Fung, former Hewlett Packard RISC project manager. (GVW: Supertek.)

W. K. Giloi's design chosen as basis for German Suprenum project. (MS: Suprenum, Giloi.)

NEC SX-2 with 1 processor achieves 46 MFLOPS on 100^2 LINPACK. (JD: Linpack Benchmark, NEC SX-2.)

Sisal 1.2 language definition released; language definition does not change for another seven years. (JF: SISAL, functional languages.)

David Gelernter publishes description of Linda language. Key elements of this later re-appear as the Linda parallel programming system. (GVW: Gelernter, Linda.)

Robert Halstead introudces futures in a paper describing the implementation of Multilisp. (GVW: Multilisp, Halstead, futures.)

David Jefferson describes how virtual time and time warping can be used as a basis for speculative distributed simulations. (GVW: Jefferson, timewarp, simulation.)

1986

Dally shows that low-dimensional k-ary n-cubes are more wire-efficient than hypercubes for typical values of network bisection, message length, and module pinout. Dally demonstrates the torus routing chip, the first low-dimensional wormhole routing component. (WD: Dally, k-ary n-cubes, hypercubes, wormhole routing.)

Kai Li describes system for emulated shared virtual memory. (GVW: Li, shared virtual memory.)

Encore ships first bus-based Multimax computer (NS32032 processors coupled with Weitek floating-point accelerators). (GVW: Encore, Multimax.)

Thinking Machines Corp. ships first Connection Machine CM-1 (up to 65536 single-bit processors connected in hypercube). (GVW: TMC, CM-1.)

Scientific Computer Systems delivers first SCS-40, a Cray-compatible minisupercomputer. (GVW: SCS.)

GE installs a prototype 10 processor Warp system at CMU (programmable bit-slice VLIW systolic array). (JRR: CMU, GE, Warp.)

Cray X/MP with 4 processors achieves 713 MFLOPS (against a peak of 840) on 1000^2 LINPACK. (JD: Linpack Benchmark, Cray X/MP.)

Floating Point Systems introduces T-series hypercube (Weitek floating-point units coupled to transputers), and ships 128-processor system to Los Alamos. (BRC: FPS, T-series, transputer.)

Henry Burkhardt, former Data General and Encore founder, forms Kendall Square Research Corporation (KSR) to build custom multiprocessor. (GVW: KSR.)

BBN forms Advanced Computers Inc. subsidiary (BBN ACI) to develop and market Butterfly machines. (GVW: BBN.)

Active Memory Technology spun off from ICL to develop DAP products. (GVW: AMT, ICL, DAP.)

Level 2 BLAS activity started. (JD: Level 2 BLAS.)

CrOS III, Cubix (file-system handler) and Plotix (graphics handler) running on Caltech hypercubes. (GVW: hypercube, MPI.)

Symmetric multiprocessing supported by VMS. (JMF: DEC, symmetric multiprocessor, VAX.)

1987

ETA produces first air- and liquid nitrogen-cooled versions of ETA^{10} multiprocessor supercomputer. (GVW: ETA.)

Myrias produces prototype (68000-based) SPS-1. (GVW: Myrias, SPS-1.)

Caltech Mark III hypercube completed (68020 with wormhole routing). (GVW: Caltech, hypercube.)

Cydrome delivers first Cydra 5 system in September. System is a multiprocessor, with a single VLIW-style numeric processor for numeric applications, plus multiple scalar processors for I/O and other general-purpose processing. Numeric processor has a 256-bit instruction word capable of 7 operations per cycle. (RR: Cydrome, VLIW.)

TMC introduces CM-2 Connection Machine (64k single-bit processors connected in hypercube, plus 2048 Weitek floating point units). (GVW: TMC, CM-2.)

Sequent produces 80386-based Symmetry bus-based multiprocessor. (GVW,TL: Sequent, Symmetry.)

Multiflow delivers first Trace/200 VLIW machines (256 to 1024 bits per instruction). (GVW: Multiflow, Trace/200.)

GE installs the first 10-processor production Warp system at CMU. (JRR: CMU, GE, Warp.)

Seitz, working at Ametek, builds the Ametek-2010, the first parallel computer using a 2-D mesh interconnect with wormhole routing. (WD: Seitz, Ametek, Ametek-2010, wormhole routing.)

Steve Chen leaves Cray Research to found Supercomputer Systems, Inc. SSI is later funded by IBM to build large-scale parallel supercomputer. (MW: CRI, SSI.)

Gordon Bell Prize for parallel performance first awarded; recipients are Brenner, Gustafson, and Montry, for a speedup of 400-600 on variety of applications running on a 1024-node nCUBE; and Chen, DeBenedictis, Fox, Li, and Walker, for speedups of 39-458 on various hypercubes. (GVW: Gordon Bell Prize.)

ETA 10 with 1 processor achieves 52 MFLOPS on 100^2 LINPACK; NEC SX-2 with 1 processor achieves 885 MFLOPS (against a peak of 1300) on 1000^2

LINPACK. (JD: Linpack Benchmark, ETA 10, NEC SX-2.)

SC (SISAL Compiler) released by LLNL and Colorado State University. First functional language, native-code compiler and runtime system for shared-memory multiprocessor systems. (JF: SISAL, functional languages.)

ParaSoft spun off from hypercube group at Caltech to produce commercial version of CrOS-like MPI. (GVW: Express, ParaSoft, hypercube, MPI.)

1988

John Gustafson and others demonstrate that Amdahl's Law can be broken by scaling up problem size. (GVW: scalability, Gustafson.)

Inmos produces first T800 floating-point transputer; Parsys and Telmat set up to exploit results of ESPRIT Supernode project, and begin marketing T800-based machines. (GVW: Inmos, transputer.)

Silicon Graphics delivers the Power Series graphics workstations (bus-based multiprocessor workstations and servers with up to 8 MIPS R2000 RISC microprocessors). (DS: Silicon Graphics, Power Series.)

CRI produces first Y/MP multiprocessor vector supercomputer. (GVW: CRI, Cray-Y/MP.)

AMT delivers first re-engineered DAP (1024 single-bit processors connected in torus). (GVW: AMT, DAP.)

Convex introduces second-generation C2 mini-supercomputers. (DHS: Convex, C2.)

Intel produces iPSC/2 hypercube (80386/7 chip-set with wormhole routing, plus concurrent I/O facilities). (GVW: Intel, iPSC/2.)

Ardent and Stellar begin delivering single-user graphics engineering workstations. (GVW: Stellar, Ardent.)

Hitachi ships first S-820 vector supercomputer. (YO: Hitachi, S-820.)

Definition of Occam2 concurrent programming language published. (RS: Occam.)

The 128 processing-element SIGMA-1 dataflow machine of Japan's Electro-Technical Laboratory (ETL) delivers over 100 MFLOPS. (PGW: dataflow, SIGMA-1, ETL.)

Floating Point Systems Inc. changes name to FPS Computing, buys Celerity Computing assets, and produces Model 500 (Celerity 6000) mini-supercomputer with multiple scalar and vector processors. (BRC: FPS, Celerity.)

MasPar Computer Corp. founded by former DEC executive Jeff Kalb to develop bit-serial massively-parallel machines. (MW: DEC, MasPar.)

Cydrome closes doors in December due to financial problems. (RR: Cydrome.)

Tera Computer Co. founded by Burton Smith and James Rottsolk to develop and market a new multi-threaded parallel computer, similar to the Denelcor HEP. (LSK: Tera.)

Scalable Coherent Interface (SCI) working group formed to develop standard for interconnection network providing 1 GByte per second per processor and cache coherence using many unidirectional point-to-point links. (DBG: SCI.)

Cray Y/MP with 1 processor achieves 74 MFLOPS on 100^2 LINPACK; the same machine with 8 processors achieves 2.1 GFLOPS (against a peak of 2.6) on 1000^2 LINPACK. (JD: Linpack Benchmark, Cray Y/MP.)

Gordon Bell Prize awarded to Vu, Simon, Ashcraft, Grimes, and Peyton, whose static structures program achieved 1 GFLOPS on an 8-processor Cray Y/MP. (GVW: Gordon Bell Prize.)

Level 2 BLAS published/released; Level 3 BLAS activity started; LAPACK project started. LAPACK effort to produce software for linear algebra problems on shared memory parallel computers and high-performance workstations. (JD: Level 2 BLAS, Level 3 BLAS, LAPACK.)

ParaSoft releases first commercial version of Express MPI; first version of DIME (Distributed Irregular Mesh Environment) up and running at Caltech. (GVW: ParaSoft, Express, MPI, Caltech, DIME.)

1989

Valiant argues that random routing and latency hiding can allow physically-realizable machines to emulate PRAMs in optimal time. (GVW: Valiant, random routing, PRAM, emulation.)

Scientific Computer Systems stops selling its SCS-40 Cray-compatible computer system. SCS continues to sell high-speed token ring network. (MW: SCS.)

BBN ACI delivers first 88000-based TC2000 distributed shared-memory multiprocessor. (GVW: BBN, TC2000.)

Myrias sell first 68020-based SPS-2 shared-memory multiprocessor. (GVW: Myrias, SPS-2.)

Meiko begin using SPARC and Intel i860 processors to supplement T800s in their Computing Surface machines; begins integrating products with SunOS enviornment. (GVW: Meiko, Computing Surface.)

Evans and Sutherland announce the ES-1 parallel computer. Two systems are delivered, to the University of Colorado and CalTech. The division is later shut down during the Supercomputing '89 conference, even while they had a booth in the convention center in Reno. (MW: ES-1.)

Multiflow produces second-generation Trace/300 machines. (MW: Multiflow, Trace/300.)

Fujitsu begins production of single-processor VP2000 vector supercomputers. (GVW: Fujitsu, VP2000.)

Supertek Computers, Inc., delivers its S-1 Cray-compatible minisupercomputer; eventually 10 of these are sold. (MW: Supertek.)

Control Data shuts down ETA Systems in April; National Science Foundation subsequently shuts down the John von Neumann Supercomputer Center at Princeton, which was operating an ETA-10. (MW: CDC, ETA.)

Stellar and Ardent announce they will merge, forming Stardent Computers. (MW: Stellar, Ardent, Stardent.)

Seymour Cray leaves Cray Research to found Cray Computer Corporation. (GVW: CRI, CCC.)

Arvind's group at MIT receives first hardware prototype of MONSOON tagged-token architecture from Motorola. (PGW: Monsoon, dataflow, Motorola, MIT, Arvind.)

Gordon Bell Prize for absolute performance awarded to a team from Mobil and Thinking Machines Corporation, who achieved 6 GFLOPS on a CM-2 Connection Machine; prize in price/performance category awarded to Emeagwali, who achieved 400 MFLOPS per million dollars on the same platform. (GVW: Gordon Bell Prize.)

Cray Y/MP with 8 processors achieves 275 MFLOPS on 100^2 LINPACK, and 2.1 GFLOPS (against a peak of 2.6) on 1000^2 LINPACK. (JD: Linpack Benchmark, Cray Y/MP.)

OSC (Optimizing SISAL Compiler) released by LLNL and CSU. The compiler optimizes the copy and memory management; SISAL programs achieve Fortran speeds on conventional shared-memory multiprocessors. (JF: SISAL, functional languages.)

nCUBE produces second-generation nCUBE/2 hypercubes, again using custom processors. (MW: nCUBE, nCUBE/2.)

The Portland Group (PGI) founded to develop software pipelining compilers for the Intel i860 and other machines. (LFM: Portland Group.)

1990

Multiflow closes doors in April after several deals with other companies fall through. (MW: Multiflow.)

First MasPar MP-1 delivered (up to 16k 4-bit processors connected in 8-way mesh). (GVW: MasPar, MP-1.)

NEC ships SX-3, the first Japanese parallel vector supercomputer (up to 4 processors, each with up to 4 pipeline sets, a 2.9 ns clock, and up to 4 Gbyte of memory). (PDT: NEC, SX-3.)

Fujitus ships first VP-2600 vector supercomputer. (YO: F, u, j, i, t, s, u, ,, V, P, -, 2, 6, 0, 0.)

Alliant delivers first FX/2800 i860-based multiprocessors. (GVW: Alliant, FX/2800.)

In a project led by MITI, Fujitsu, Hitachi, and NEC build a testbed parallel vector supercomputer containing four Fujitsu VP2600s, NEC's shared memory, and Hitachi software. (OY: Fujitsu, NEC, Hitachi, HPPS.)

Intel produces iPSC/860 hypercubes, using i860 microprocessor and wormhole-routed connections. (RJ: Intel, iPSC/860.)

Intel demonstrates iWarp system to CMU and DARPA (descendent of Warp, with custom microprocessor replacing wire-wrapped boards). (JRR: Intel, iWarp.)

Wavetracer builds the DTC (Data Transport Computer) consisting of one to four boards of 16×16×16 1-bit PEs, virtual array size, first three-dimensional array processor. (MCS: Wavetracer, DTC.)

Cray Research, Inc., purchases Supertek Computers Inc., makers of the S-1, a minisupercomputer compatible with the Cray X-MP. (MW: Cray, Supertek.)

MIT J-Machine demonstrates message-driven network interface that reduces overhead of message handling. (WD: Dally, J-Machine, Actors model.)

National Energy Research Supercomputer Center (NERSC) places order with Cray Computer Corporation for Cray-3 supercomputer. The order includes a unique 8-processor Cray-2 computer system that is installed in April. (MW: CCC, Cray-3, NERSC.)

University of Tsukuba completes 432 processor machine QCDPAX in collaboration with Anritsu Corporation. (YO: QCDPAX, Anritsu.)

The two ETA-10 systems at the closed John von Neumann Supercomputer Center are destroyed with sledge hammers, in order to render them useless, after no buyers are found. (MW: ETA.)

Gordon Bell Prize in price/performance category awarded to Geist, Stocks, Ginatempo, and Shelton, who achieved 800 MFLOPS per million dollars in a high-temperature superconductivity program on a 128-node Intel iPSC/860; prize in compiler parallelization category awarded to Sabot, Tennies, and Vasilevsky, who achieved 1.5 GFLOPS on a CM-2 Connection Machine with Fortran 90 code derived from Fortran 77. (GVW: Gordon Bell Prize.)

Fujitsu VP2600 with 1 processor achieves 2.9 GFLOPS (against a peak of 5 GFLOPS) on 1000^2 LINPACK. (JD: Linpack Benchmark, Fujitsu VP2600.)

Level 3 BLAS published/released. The Parallel Virtual Machine (PVM) project started. PVM is designed to develop a software layer needed to put together a heterogeneous collection of computers hooked together by a network to be used as a single large parallel computer. Proof of concept software produced (PVM 1.0 not publicly released). (JD: Level 3 BLAS, PVM.)

Applied Parallel Research (APR) spun off from Pacific-Sierra Research (PSR) to develop FORGE and MIMDizer parallelization tools, and upgrade them to handle Fortran 90. (BMB: APR, FORGE, MIMDizer, PSR.)

TMC and AMT sign co-operative agreement to standardize languages. (1990: data-parallel languages, TMC, AMT.)

1991

Abhiram Ranade describes how message combining, butterfly networks, and a complicated routing algorithm can emulate PRAMs in near-optimal time. (GVW: Ranade, butterfly, PRAM, emulation.)

Myrias closes doors. (GVW: Myrias.)

BBN shuts down its Advanced Computers, Inc. (ACI) subsidiary, though it continues to sell TC-2000 computers. (MW: BBN.)

Stardent, formed by merger in 1989, announces it will sell off its business and shut its doors. The graphics computer line (the former Ardent architecture) is eventually taken over by Kubota Pacific Computer Corp. (MW: Stardent.)

CRI produces first Y/MP C90. (GVW: CRI, Cray-Y/MP C90.)

Convex ships first C3 supercomputer based on gallium arsenide (GaAs). (DHS: Convex, C3.)

Kendall Square Research starts to deliver 32-processor KSR-1 computer systems. (MW: KSR.)

Thinking Machines Corporation produces CM-200 Connection Machine, an upgraded CM-2. MIMD CM-5 announced. (BMB: TMC, CM-200.)

64-processor nCUBE 2 with 48 I/O processors and 205 disks achieves 1073 transactions per second running Oracle Parallel Server — twice the speed of the fastest contemporary mainframe, at one twentieth the cost per transaction. (JB,VK: nCUBE, Oracle Parallel Server.)

Cray Y/MP C90 with 16 processors achieves 403 MFLOPS on 100^2 LINPACK; a Fujitsu VP2600 with 1 processor achieves 4 GFLOPS (against a peak of 5 GFLOPS) on 1000^2 LINPACK. (JD: Linpack Benchmark, Cray Y/MP C90, Fujitsu VP2600.)

Intel introduces the iWarp system, featuring the iWarp LIW processor with on-chip integrated communication, long lived connections, systolic and low-latency communication, and 512 kbyte to 2 Mbyte per processor. (JRR: Intel, iWarp.)

Intel delivers Touchstone Delta prototype for its Paragon multicomputer (two-dimensional mesh of i860 microprocessors with wormhole routing) to the Concurrent Supercomputing Consortium at Caltech; commercial deliveries of Paragon begin late in the year. (RJ: Intel, Paragon.)

FPS Computing delivers MCP-784, an 84-processor shared memory i860-based system, uses data-vectorization into caches. (BRC: FPS, MCP-784.)

In December, the National Energy Research Supercomputer Center (NERSC) at Lawrence Livermore National Laboratory cancels contract to buy Cray-3 from Cray Computer Corp. (MW: CCC, Cray-3.)

Germany's Suprenum project produces first bug-free hardware. Machine contains nodes based on MC68020 with Weitek floating point accelerator; clusters contain 16 nodes communicating over a bus, and clusters are connected through bi-directional links. No further hardware is built, as the technology used was no longer competitive. (MS: Suprenum.)

The High Performance Fortran (HPF) forum is formed to define data-parallel extensions to Fortran. (LFM: HPF.)

OSC 12.0, released by LLNL and CSU. First functional language compiler for multiprocessor vector supercomputers. SISAL programs achieve Fortran speeds on the Cray-X/MP and Cray-Y/MP supercomputers. (JF: SISAL, functional languages.)

David Bailey publishes complaint about abuse of benchmarks, particularly by parallel computer vendors. (GVW: Bailey, benchmarking.)

Meiko produces commercial implementation of ORACLE Parallel Server RDBMS for multi-SPARC Computing Surface systems. (TA: Meiko, Computing Surface, Oracle.)

1992

Garth Gibson's thesis on redundant arrays of inexpensive disks (RAID) published. (GVW: Gibson, RAID.)

Alliant declares bankruptcy. (LFM: Alliant.)

AMT bankrupt; revived as AMT Cambridge Ltd. (MW: AMT.)

FPS Computing bankrupt; selected assets bought by CRI, and Cray Research Superservers (CRS) subsidiary formed. FPS Model 500 renamed Cray S-MP; FPS MCP renamed Cray APP. (BRC: FPS, CRI.)

Kendall Square Research announces KSR-1 after testing a system with 128 processors and a second level ring interconnect. (MW: KSR.)

MasPar Computer starts delivering its second generation machine, the MP-2. (MW: MasPar.)

Thinking Machines Corporation produces first CM-5, containing up to 1024 Sparc microprocessors connected in a fat tree topology, each with up to 4 vector units manufactured by Texas Instruments. A RAID system for the CM-5 is also announced. (BMB: TMC, CM-5.)

nCUBE introduces the nCUBE 2S family of systems based on a custom VLSI processr. (VK,JB: nCUBE, nCUBE 2S.)

Ultra III Ultracomputer prototype begins operation at New York University; first example of asynchronous message combining hardware. (AG: message combining, NYU, Ultracomputer.)

Gordon Bell Prize for absolute performance awarded to Warren and Salmon, who achieved 5 GFLOPS on the Intel Touchstone Delta in a gravitational interaction tree code; prize for speedup awarded to Jones and Plassmann, who also achieved 5 GFLOPS on the same platform. Prize for price/performance awarded to Nakanishi, Rego, and Sunderam, whose Eclipse system achieved 1 GIPS per million dollars on a widely distributed network of workstations. (GVW: Gordon Bell Prizes.)

Cray Y/MP C90 with 16 processors achieves 479 MFLOPS on 100^2 LINPACK; an NEC SX-3/44 with 4 processors achieves 13.4 GFLOPS (against a peak of 22.0) on 1000^2 LINPACK, and 20.0 GFLOPS on a 6144^2 problem. (JD: Linpack Benchmark, Cray Y/MP C90, NEC SX-3.)

LAPACK software released/users guide published. ScaLAPACK Project started, designed to provide linear algebra software on highly parallel systems. Message Passing Interface (MPI) Forum started, standardizing effort for message passing systems. (JD: LAPACK, ScaLAPACK, MPI.)

Chandy and Taylor describe PCN, a parallel programming system similar to Strand 88, based on dataflow and logic programming. (GVW: PCN, Chandy, Taylor.)

1993

IBM delivers first Powerparallel system based on RISC RS/6000 processor. (HGK: IBM, RS/6000.)

Silicon Graphics ships Challenge series of bus-based multiprocessor graphics workstations and servers, containing up to 36 MIPS R4400 RISC microprocessors. (DS: Silicon Graphics, Challenge.)

IBM stops funding of Supercomputer Systems Inc.; company shuts down. (MW: SSI.)

Cray Computer Corp. Cray-3 placed at National Center for Atmospheric Research. (EAB: CCC, Cray-3.)

Lawrence Livermore National Laboratory (LLNL) announces intention to purchase CS-2 Computing Surface from Meiko, the first major purchase by a U.S. national laboratory from a vendor with roots outside the U.S. (GVW: Meiko, LLNL.)

Fujitsu installs 140-processor Numerical Wind Tunnel, a prototype of a highly-parallel vector supercomputer to be called VPP-500. (YO: Fujitsu, VPP-500.)

NEC produces Cenju-3, containing up to 256 VR4400SC (MIPS R4000 run-alike) processors connected by an Omega network. (PDT: NEC, CENJU-3.)

GF-11 system (the name stands for 11 GFLOPS) purpose-built at IBM for quantum chromodynamic calculations finishes computation of nucleon masses. (HGK: IBM, GF-11.)

512-node J-Machines (message-driven multicomputers) operational at MIT and Caltech. (WD: J-Machine, MIT, Caltech, Actors model.)

Version 1.0 of the HPF language specific is released. (LFM: HPF.)

An NEC SX-3/44 with 4 processors achieves 15.1 GFLOPS (against a peak of 25.0) on 1000^2 LINPACK; a Thinking Machines Corporation CM-5 achieves 59.7 GFLOPS with 1024 processors on a 52224^2 problem. (JD: Linpack Benchmark, NEC SX-3, CM-5.)

ScaLAPACK Prototypes released, runs on Intel's Paragon, Thinking Machines' CM-5, and PVM. PVM 3.0 publicly available. (JD: ScaLAPACK, PVM.)