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PROFESSIONAL TIMELINE

Associate Research Specialist (1993–present), **Visiting Postdoctoral Computer Scientist** (1991–1993), University of California at Berkeley, Computer Science Division.

Visiting Associate, California Institute of Technology, (1994–present).

Research Assistant Professor, University of Colorado at Boulder, Department of Electrical and Computer Engineering (1990–1991).

Graduate Education: California Institute of Technology, Ph.D., Computer Science, June 1990, M.S., Computer Science, June 1986. Research Advisor: Carver Mead.

Undergraduate Education: University of Pennsylvania, B.S., Electrical Engineering, B.S., Computer Science, May 1984.

MAJOR RESEARCH FOCUS

My research concerns the design of real-time, low-power analog VLSI systems to model biological auditory processing, and the engineering applications of these implementations. My graduate years at Caltech focused on the basic research for this technology. We (Carver Mead, Richard Lyon, and I) designed a series of analog integrated circuits that modeled pitch perception, auditory localization, and spectral shape perception, as a proof of concept for the implementation techniques.

At Berkeley, we (John Wawrzynek and I) have focused on using these analog circuit blocks in engineering applications. Together with other collaborators, we have developed interface technologies that support the efficient use of analog auditory pre-processors in digital systems. The result of this research is a special-purpose analog-to-digital converter chip: the chip receives an analog audio input, performs a variety of biologically-motivated analog signal processing operations (under digital control), and communicates the final representation off-chip using an efficient digital encoding.

Presently, we have a working system with several of these converter chips, interfaced to a workstation, that functions as a real-time visualization system for auditory representations. For the past year, we have been actively using this system in conjunction with speech recognition software, to efficiently explore different combinations of auditory representations as speech recognition front-ends.

Our current focus is the construction of complete systems using these analog circuit blocks that consume a few microwatts of power: these systems consume as much power during operation as low-power digital signal processing systems consume in "sleep mode." Applications of analog micropower systems include speech recognition systems that could operate on a wristwatch battery for several years, and signal-based power managers for digital systems.

The Web site *http://www.cs.berkeley.edu/ lazzaro/siau.html* describes this research in more detail.

OTHER RESEARCH PROJECTS

For the past four years, I have served on the management team of T0, a digital vector microprocessor project at Berkeley. I participated in weekly design review meetings, and reviewed project reports (but did no actual design), as the chip progressed through several architectural redefinitions, final architecture freeze, circuit schematic freeze, layout freeze, tapeout, successful first silicon, and successful prototype board operation.

The 750,000 transistor chip, full reticle (16mm by 17mm) on HP's 1 micron CMOS process, runs at 40 MHz, and performs its intended application (backpropagation training of large neural networks) over 20 times faster than a Sparc 20.

The Web site *http://www.icsi.berkeley.edu/real/spert/t0-intro.html* describes this research in more detail.

For my Master's thesis at Caltech, I designed and implemented **ana**, a functional simulator for analog VLSI circuits. The program, about 35,000 lines of C source code running under the X Window System, works in conjunction with the schematic editor LOG. Together, ana and LOG implement a simulated laboratory bench, where system topology and parameter values can be altered without stopping a simulation. I actively maintain the system, and distribute it via the Internet (http://www.pcmp.caltech.edu/chipmunk/) and CD-ROM compilation disks to hundreds of users worldwide.

TEACHING EXPERIENCE

Instructor, UC Berkeley (Spring 1994): Instructor for an introductory graduate-level course, VLSI Systems Design (CS250), based on the Weste and Eshraghian text.

PROFESSIONAL SERVICE

Tutorial Chair, Neural Information Processing Systems (NIPS) Conference, 1996.

Treasurer, Neural Information Processing Systems (NIPS) Conference, 1995.

Member, International Advisory Board, Sixth Australian Conference On Neural Networks (ACNN 95).

Member, Scientific Committee, Neurapply 95, France.

Implementations Area Chair, Neural Information Processing Systems (NIPS) Conference, 1993 and 1994. I selected reviewers and made final accept/reject recommendations for implementations papers.

Tutorial Presenter, Neural Information Processing Systems (NIPS) Tutorial, 1993. Presented a 2-hour tutorial on VLSI Implementations, and prepared a 100-page tutorial booklet (bibliography and selected papers) for the attendees.

JOURNAL PUBLICATIONS

Lazzaro, J., Wawrzynek, J., Lippmann, R. P. (1997). A micropower analog circuit implementation of hidden markov model state decoding. *IEEE Journal Solid State Circuits* **32**:8, 1200–1209.

Lazzaro, J. P., Wawrzynek, J. (1997). Speech recognition experiments with silicon auditory models. *Analog Integrated Circuits and Signal Processing,* **13**:1-2, 37-51.

Lazzaro, J. P., Wawrzynek, J. (in press). Speech recognition experiments with silicon auditory models. *Analog VLSI and Signal Processing.*

Lazzaro, J. P., Wawrzynek, J., and Kramer, A (1994). Systems technologies for silicon auditory models. *IEEE Micro*, **14**:3. 7-15.

Lazzaro, J. P., Wawrzynek, J., Mahowald., M., Sivilotti, M., Gillespie, D. (1993). Silicon auditory processors as computer peripherals. *IEEE Journal of Neural Networks* **4**:3 523–528.

Horiuchi, T., Bair, W., Bishofberger, B., Moore, A., Koch, C., Lazzaro, J. (1992). Computing motion using analog VLSI chips - an experimental comparison among different approaches. *International Journal of Computer Vision* **8**:3, 203-216.

Lazzaro, J. P. (1991). A silicon model of an auditory neural representation of spectral shape. *IEEE Journal Solid State Circuits* **26**: 772–777.

Mead, C. A., Arreguit, X., and Lazzaro, J. P. (1991). Analog VLSI models of binaural hearing. *IEEE Journal of Neural Networks* **2**: 230–236.

Lazzaro, J. and Mead, C. (1989). Silicon modeling of pitch perception. *Proceedings National Academy of Sciences* **86**: 9597–9601.

Lazzaro, J. and Mead, C. (1989). A silicon model of auditory localization. *Neural Computation* **1**: 41–70.

CONFERENCE PUBLICATIONS (COMPETITIVE)

Lazzaro, J. P., Wawrzynek J., and Lippmann, R. (1996). A micropower analog VLSI HMM state decoder for wordspotting. In Jordan, M., Mozer, M., and Petsche, T. (eds), *Advances in Neural Information Processing Systems 9.* Cambridge, MA: MIT Press.

Lazzaro, J. P., Wawrzynek J. (1995). Silicon models for auditory scene analysis. In Mozer, M., Touretsky, D., and Hasselmo, M. (eds), *Advances in Neural Information Processing Systems 8.* Cambridge, MA: MIT Press.

Lazzaro, J. P. and Wawrzynek, J. (1995). A multi-sender asynchronous extension to the address-event protocol. In Dally, W. J., Poulton, J. W., Ishii, A. T. (eds), *16th Conference on Advanced Research in VLSI,* pp. 158–169.

Lazzaro, J. P., Wawrzynek, J., Mahowald., M., Sivilotti, M., Gillespie, D. (1993). Silicon auditory processors as computer peripherals. In Hanson, S., Cowan, J., and Giles C., (eds), *Advances in Neural Information Processing Systems 5.* San Mateo, CA: Morgan Kaufmann Publishers, 820–827.

Lazzaro, J. P. (1992). Temporal adaptation in a silicon auditory nerve. In Moody, J., Hanson, S., Lippmann, R. (eds), *Advances in Neural Information Processing Systems 4.* San Mateo, CA: Morgan Kaufmann Publishers, pp 813–820.

Lazzaro, J. P., Schwaber, J., and Rogers, W. (1991). Silicon baroreceptors: modeling cardiovascular pressure transduction in analog VLSI. In Sequin, C. (ed), *Advanced Research in VLSI, Proceedings of the 1991 Santa Cruz Conference,* Cambridge, MA: MIT Press, pp. 163–177.

Horiuchi, T., Lazzaro, J. P., Moore, A., and Koch, C. (1991). A correlation-based motion detection chip. In Lippman, R., Moody, J., Tourestzky, D. (eds), *Advances in Neural Information Processing Systems 3.* San Mateo, CA: Morgan Kaufmann Publishers, 406–413.

Lazzaro, J., Ryckebusch, S., Mahowald, M. A., and Mead, C. (1988). Winner-take-all networks of O(n) complexity. In Tourestzky, D. (ed), *Advances in Neural Information Processing Systems 1.* San Mateo, CA: Morgan Kaufmann Publishers, pp. 703-711.

Mueller, P. and Lazzaro J. (1986). A machine for neural computation of acoustical patterns with applications to real-time speech recognition. In Denker, J. (ed), *Neural Networks for Computing (Snowbird, Utah).* American Institute of Physics Conference Proceeding 151, pp. 321-327.

CONFERENCE PUBLICATIONS (INVITED)

Lazzaro, J. P., Wawrzynek, J., and Kramer, A (1994). Systems technologies for silicon auditory models. *Fall Meeting of the Biomedical Engineering Society,* published in the abstract supplement to the *Annals of Biomedical Engineering,* **22**:1, p. 53.

Lazzaro, J. P. (1992). Low-power silicon spiking neurons and axons. *IEEE International Symposium on Circuits and Systems* San Diego, CA, pp. 2220-2224.

Lazzaro, J. P. (1991). Biologically-based auditory signal processing in analog VLSI. *IEEE Asilomar Conference on Signals, Systems, and Computers*, pp. 790-794.

BOOK CHAPTERS

Lazzaro, J. P., and Wawrzynek, J. (1994). Low-power silicon axons, neurons, and synapses. In Zaghloul, M. E., Meador, J. L., and Newcomb, R. W., (eds) *Silicon Implementations of Pulse Coded Neural Networks.* Norwell, MA: Kluwer Academic Publishers, pp. 153-164.

Lazzaro, J. and Mead, C. (1990). Silicon models of auditory localization. In Zornetzer, Davis, and Lau (eds), *An Introduction to Neural and Electronic Networks.* New York: Academic Press, pp. 158–174.

Lazzaro, J. and Mead, C. (1989). Circuit models of sensory transduction in the cochlea. In Mead, C. and Ismail, M. (eds), *Analog VLSI Implementations of Neural Networks.* Norwell, MA: Kluwer Academic Publishers, pp. 85-101.