Homework 3 Solutions

CIS 501, Spring 1998
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1. Exercise 2.2, pg 119.

   $CPUtime = CPI \times \#instr \times Clock\,Cycle$

   $CPUtime_{new} = CPUtime_{old}$

   $CPI \times ((100\% - 22.8\%) + x) \times 1.1 \times Clock\,Cycle = CPUtime = CPI \times 100\% \times Clock\,Cycle$

   $x = 13.7\%$

   $\frac{(22.8\% - 13.7\%)}{22.8\%} = 39.9\%$
   39.9% of the loads must be eliminated.

   The following two instructions can not be replaced:

   Load R1, 0(Rb)
   Add R2, R1, R1

2. Exercise 2.3, pg 120.

   (a) Accumulator

   Load B Add C Store A
   Add C Store B
   Load A Sub B Store D

   Instruction bytes fetched: $(1+2) \times 8 = 24$
   Memory-data bytes transferred: $4 \times 8 = 32$
   Total: 56

   (b) Memory-Memory

   Add A B C
   Add B A C
   Sub D A B

   Instruction bytes fetched: $(1+2+2+2) \times 3 = 21$
   Memory-data bytes transferred: $(4+4+4) \times 3 = 36$
   Total: 57

   (c) Stack

   Push B Push C Add Pop A
   Push A Push C Add Pop B

Push A Push B Sub Pop D

Instruction bytes fetched: $(1+2) \times 9 + 1 \times 3 = 30$
Memory-data bytes transferred: $4 \times 3 \times 3 = 36$
Total: 66

(d) Load-Store

Load R1, B Load R2, C Add R3, R1, R2 Store A, R3
Add R1, R3, R2 Store B, R1
Sub R2, R3, R1 Store D, R2

Instruction bytes fetched: Register specifiers are 1/2 bytes long. Therefore Load-Store instructions are 1+1/2+2 = 3 1/2 = 4 bytes. Similarly, Add-Subs are 1+1/2+1/2+1/2 = 2 1/2 = 3 bytes. So total is $4 \times 5 + 3 \times 3 = 29$
Memory-data bytes transferred: $4 \times 5 = 20$
Total: 49

As shown above, the Memory-Memory architecture is more efficient measured by code size, and Load-Store is more efficient measured by memory bandwidth.

3. Exercise 2.6, pg 121.

```
        SW      R0, 2000(R0)    i = 0;
LOOP:   LW      R1, 2000(R0)    R1 = i;
        SUBI    R2, R1, #101    i == 101?
        BEQZ    R2, EXIT
        LW      R3, 1500(R0)    R3 = C;
        MULTI   R4, R1, #4      R4 = i*4;
        LW      R5, 5000(R4)    R5 = B[i];
        ADD     R6, R5, R3      R6 = B[i] + C;
        SW      R6, 0(R4)       A[i] = B[i] + C;
        ADDI    R1, R1, #1      i++;
        SW      R1, 2000(R0)    store i;
        J       LOOP
EXIT:
```

Loop is executed 101 times therefore there are $101 \times 11 + 1 = 1112$ instructions. There are $5 \times 101 + 1 = 506$ memory references. Code size in bytes is $12 \times 4 = 48$

4. Exercise 2.12, pg 122.

$\frac{IC_{new}}{IC_{old}} = \frac{(1-0.25-0.9) \times IC_{old} + 0.9 \times (0.26+0.9) \times IC_{old}}{IC_{old}} = 96.5\%$

$CPUtime = CPI \times \#instr \times Clock\ Cycle$
$CPUtime_{new} = CPI_{old} \times 0.965 IC_{old} \times 1.05 ClockCycle_{old} = 1.013 \times CPUtime_{old}$
Thus, the original machine is 1.013 times faster than the enhanced machine.