Homework 4

CIS 501, Spring 1998
Due on February 18, 1998

1. A machine is called "underpipelined" if additional levels of pipelining can be added without changing the pipeline-stall behaviour appreciably. Suppose that the DLX integer pipeline was changed to four stages by merging EX and MEM and lengthening the clock cycle by 50%. How much faster would the conventional DLX pipeline be versus the underpipelined DLX on integer code only? Assume that the number of stalls goes down from 9% to 5%.

2. Consider the following code fragment:

```
LW      R3, 0(R2)
ADD     R1, R2, R3
ADD     R4, R1, R1
SUB     R2, R3, R2
```

   Assume a simple, pipelined DLX. Assume that each stage of the pipeline takes 1 clock cycle. Write out a diagram similar to that of Figure 3.14 showing the execution of these instructions for each of the following cases:

   (a) Assume that any data hazads cause a stall in the pipeline and that there are no mecahnisms for forwrding results. Do assume that the register set is written in the first half of a cycle and read in the second half.

   (b) Assume now that forwarding of results is available.

   (c) Assume that the memory path is shared by both instruction fetches as well as data accesses so that there is a structural hazard. Further assume that the forwarding of results is available.

   In each case calculate the total number of clock cycles required to execute the fragment.

3. Take the following code:

```
loop:   LW      R1, 0(R2)
        ADDI    R1, R1, \#1
        SW      R1, 0(R2)
        ADDI    R2, R2, \#4
        SUB     R4, R3, R2
        BNZ     R4,loop
```

   Use the DLX pipeline. Assume that the branch causes the pipeline to be flushed, and that the register set is written in the first half of a cycle and read in the second.

   The initial value of R3 is R2 + 396

   (a) Show the timing of this instruction sequence for two loop cycle without any forwarding.

   (b) Now assume that forwarding is available.

   How many clock cycles does it take to execute the entire loop in each case?