Homework 8

CIS 501, Spring 1998
Due on April 15, 1998

1. You purchase an Acme computer with the following features:
   - 95% of all memory accesses are found in the cache.
   - Each cache block is two words, and the whole block is read on any miss.
   - The processor sends references to its cache at the rate of 10^9 words per second.
   - 25% of those references are writes.
   - Assume that the memory system can support 10^9 words per second, reads or writes.
   - The bus reads or writes a single word at a time (the memory system cannot read or write two words at once).
   - Assume at any one time, 30% of the blocks in the cache have been modified.
   - The cache uses write allocate on a write miss.

   You are considering adding a peripheral to the system, but you want to know how much o fthe memory system bandwidth is already used. Calculate the percentage of memory system bandwidth used on the average in the two cases below. Be sure to state your assumptions, if any.

   (a) The cache is write through.

   (b) The cache is write back.

2. You are comparing the performance of different caches on a DLX machine. Use Figure 5.9, page 391, to obtain the miss rates for various types of caches. Unless otherwise stated, assume that
   - Loading (or storing) a cache line from main memory into cache takes 15 cycles to read (write) the first (4 byte) word, and one cycle for each additional word in the cache line (block).
   - Cache hit time is one cycle.
   - Unless otherwise stated for a particular problem, memory can deliver at most one word per cycle.
   - Initially, all lines in the cache are clean.
   - A write-through cache writes only the modified word back to memory, rather than the whole cache line.

   (a) One option is a direct-mapped 4K cache with each cache line (block) 32 bytes long. What is the miss rate for this cache? What is the average memory access time for this cache?

   (b) Another option is to double the size of the cache. You want to decide whether the new cache should be 8K/1-way or 8K/2-way. What are the average memory access times of these two caches?

   (c) After evaluating the above mentioned caches, you decide to improve the cache fill time. By organizing the memory into four banks, your new configuration allows you to read 4 words per cycle instead of just the one previously. In addition, you double the width of the cache from 32 bytes per cache line to 64 bytes per cache line. However, the first group of words still takes 15 cucles to arrive. What is the average memory access time for this cache?

   (d) Suppose you perform two writes to the cache that modify lines A and B in the cache (A and B are not in the same set in the 2-way case). Further, suppose that another line is loaded in from main memory into the cache and this line maps *into the same set as line A*. Note that for the 1-way case, the set with line A consists of only line A whereas in the 2-way case the set contains the line A as well as one more line.

      i. How long will the entire process take (in cycles) on a direct-map (1-way) write-through cache?

      ii. How long will the entire process take (in cycles) on a 2-way write-through cache?

      iii. How long will the entire process take (in cycles) on a direct-map write-back cache?

      iv. How long will the entire process take (in cycles) on a 2-way write-back cache?